Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1 – 9: Cancelled

10. (New) A circuit arrangement for bridging high voltages using a switching signal, comprising:

a voltage transmitter with first and second terminals for a low voltage;

a voltage receiver with third and fourth terminals for a higher voltage relative to the low voltage between the first and second terminals, wherein the voltage transmitter and the voltage receiver each comprise a first inverter circuit and a second inverter circuit,

wherein the inverter circuits of the voltage transmitter are connected between the first and second terminals and the inverter circuits of the voltage receiver are connected between the third and fourth terminals,

wherein an outlet of the first inverter circuit of the voltage transmitter is connected via a first capacitor as a high voltage capacitor with an inlet of the second inverter circuit of the voltage receiver and an outlet of the first inverter circuit of the voltage receiver, and an outlet of the second inverter circuit of the voltage transmitter is connected via a second capacitor as a high voltage capacitor with an inlet of the first inverter circuit of the voltage receiver and an outlet of the second inverter circuit of the voltage receiver,

wherein the inlets of the first inverter circuit and the second inverter circuit, respectively, of the voltage transmitter are a non-inverted and an inverted inlet, and wherein the outlets of the first inverter circuit and the second inverter circuit, respectively, of the voltage receiver represent outlet nodes.

11. (New) The circuit arrangement of claim 10, wherein a third inverter circuit is connected between the first and second terminals, wherein an outlet of the third inverter circuit is connected with the inlet of the first inverter circuit of the voltage transmitter, wherein the inlet of the third inverter circuit is connected with the inlet of the second inverter circuit of the voltage transmitter, and wherein the inlet of the third inverter circuit is connected with a terminal IN as the inlet of the circuit arrangement for bridging high voltages with a switching signal.

12. (New) The circuit arrangement of claim 10, wherein a fourth inverter circuit and a fifth inverter circuit are connected between the third and fourth terminals, wherein an inlet of the fourth inverter circuit is connected with the inlet of the first inverter circuit of the voltage receiver, wherein an inlet of the fifth inverter circuit is connected with the inlet of the second inverter circuit of the voltage receiver, wherein an outlet of the fourth inverter circuit is connected with a terminal OUT1 as the first outlet of the voltage receiver, and wherein an outlet of the fifth inverter circuit is connected with a terminal OUT2 as the second outlet of the voltage receiver.

13. (New) The circuit arrangement of claim 10, wherein a sixth inverter circuit and a seventh inverter circuit are connected between the first and second terminals, wherein an inlet of the seventh inverter circuit is connected with the inlet of the third inverter circuit and with a terminal IN as the inlet of the circuit arrangement for bridging high voltages with a switching signal, wherein an outlet of the seventh inverter circuit is connected with an inlet of the sixth inverter circuit, and wherein an outlet of the sixth inverter circuit is connected with the inlet of the second inverter circuit of the voltage transmitter.

14. (New) The circuit arrangement of claim 10, wherein an inverter circuit comprises two complementary transistors connected in series.

15. (New) The circuit arrangement of claim 10, wherein the first capacitor and the second capacitor are connected between the voltage transmitter and the voltage receiver in such a way that the first capacitor and the second capacitor, respectively, are charged as high voltage

capacitors to voltage differential to be overcome between the voltage transmitter and the voltage receiver and the charges of the first capacitor and second capacitor subsequently vary at a value $\Delta Q = C \times (Vdd - Vss)$ for signal transmission, wherein power consumption of the circuit arrangement for bridging high voltages with a switching signal is independent from the voltage differential to be overcome between the voltage transmitter and the voltage receiver, and wherein simultaneously, the applied differential principle guarantees a high signal-to-noise ratio relative to push-push interference signals.

16. (New) The circuit arrangement of claim 10, wherein the circuit arrangement for bridging high voltage with a switching signal is realized as an integrated semi-conductor circuit made with semi-conductor processes with CMOS circuits as the inverter circuits or a stack of layers with alternating layers of circuit stopper implantation, field oxide, poly-silicon, CVD-oxide, metal, CVD-oxide, metal, and so on, whereby the layers are electrically alternatingly connected, as the first capacitor and as the second capacitor, respectively, as high voltage capacitors.

17. (New) The circuit arrangement of claim 10, wherein the voltage transmitter is one region or multiple regions of a semi-conductor chip, wherein the first capacitor is one region and the second capacitor is one region of the semi-conductor chip, wherein the voltage receiver is one region of the semi-conductor chip, wherein at least the region of the voltage transmitter and of the voltage receiver, respectively, is surrounded by a trench for voltage isolation.

18. (New) The circuit arrangement of claim 10, wherein the circuit arrangement for bridging high voltages with a switching signal is realized as integrated semi-conductor circuits made with semi-conductor processes for integrated high voltage circuits with any isolation for the voltage transmitter, the high voltage capacitors, and the voltage receiver.